National Aeronautics and
Space Administration

Headquarters
Washington, DC 20546-0001

Patent Application

NPO-20535-2-CU
(NASA Docket No.)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing is the Patent Application of:

Applicant: STOICA, et al.

Inventor(s): ADRIAN STOICA and CARLOS SALAZAR-LAZARO

Entitled: EVOLUTIONARY TECHNIQUE FOR AUTOMATED SYNTHESIS OF ELECTRONIC CIRCUITS

Enclosed are:

- [X] Specification, claims, and declaration.
- [X] 4 sheets of drawing. [X] Power of Attorney
- [X] An assignment of the invention to the National Aeronautics and Space Administration.
- [ ] A license of the invention to the National Aeronautics and Space Administration.
- [ ] An international application under the PCT. *(See PCT/RO/101,XII checklist.)*

The fee has been calculated as shown below:

CLAIMS FILED							
FOR (1)	NUMBER FILED (2)		NUMBER EXTRA (3)		RATE (4)		FEE (5)
TOTAL CLAIMS	20 - 20	=	0	x	18	=	000.00
INDEPENDENT CLAIMS	4 - 3	=	1	x	86	=	86.00
BASIC FEE *(Minimum amount required)*							770.00
					TOTAL FILING FEE ▶		856.00

Please charge our Deposit Account No. 14-0116 in the amount shown as the total filing fee. The Commissioner is hereby authorized to charge an additional fee which may be required to effect the filing of this application under 37 CFR 1.16, or credit any overpayment to Deposit Account No. 14-0116.

January 26, 2004
(Date)

John H. Kusmiss
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UNDER 37 CFR 1.10 - SEPARATE PAPER

DOCKET NO.: NPO-20535-2-CU

In Re Application of: Adrian Stoica, et al.

Serial Number To be Assigned Filed Herewith

For: EVOLUTIONARY TECHNIQUE FOR AUTOMATED SYNTHESIS OF ELECTRONIC CIRCUITS

Group Art Unit Unknown Examiner Unknown

I hereby certify that this paper is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

I hereby certify that the following were placed in the envelope by me and are enclosed herewith for filing of the Patent Application:

[X] Transmittal letter (Original & 1 copy)

[X] Specification (30 pages including 6 pages of Claims), Abstract (1 page), and Drawings (4 Sheets, Figures 1-5)

[X] Letter to the Examiner (5 pages)

[X] Information Disclosure Statement (1 Page) with PTO Form 1449 (3 Pages) and 14 non-patent literature documents

[X] Declaration and Power of Attorney (Copy as filed in parent application)

[X] Assignment by Inventor to CalTech (Copy as filed in parent application) and Transmittal Letter (Original ~~& 1 copy~~)

[X] Assignment by CalTech to NASA (Copy as filed in parent application) and Transmittal Letter (Original ~~& 1 copy.~~)

[X] Nonpublication Request under 35 U.S.C. 122(b)(2)(B)(i)

[X] Return Postcard (1)

"Express Mail" mailing label number: EL 981376139 US
Date of Deposit: January 26, 2004

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NONPUBLICATION REQUEST UNDER 35 U.S.C. 122(b)(2)(B)(i)

First Named Inventor	Adrian STOICA, et al.
Title	AN EVOLVABLE CIRCUIT WITH TRANSISTOR-LEVEL RECONFIGURABILITY
Attorney Docket Number	NPO-20535-2-CU

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

January 26, 2004
Date

John H. Kusmiss
Signature

(818) 354-7770
Telephone number

John H. Kusmiss
Typed or printed name

Reg. No. 32,149

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

NASA Case No.: NPO-20535-2-CU

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of)
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Inventor: Stoica, et al.)
)
Serial No.: To be assigned)
)
Filed: Herewith)
)
For: AN EVOLVABLE CIRCUIT WITH TRANSISTOR-LEVEL RECONFIGURABILITY)

LETTER TO THE EXAMINER

(Accompanying Continuation Patent Application)

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In this continuation application, the claims that were finally rejected during prosecution of the parent application have been replaced by new claims 1-20.

The unallowed claims of the parent application were rejected over Levi in view of Sourgen and Layzell. Levi does not disclose transistor-level reconfiguration, as noted in the last official action in the parent application. Sourgen and Layzell were cited to overcome this shortcoming. Sourgen has nothing to do with evolutionary algorithms or the alteration of basic circuit topology. Sourgen's circuit is a programmable rising edge generator and never changes from being a programmable rising edge generator. Moreover, Sourgen fails to disclose any switch

between the source-drain connections of his transistors. (His switches are all bypass switches.) Layzell requires the switching of at least two or more of his switches to connect and disconnect between transistor terminals. (Such connection or disconnection is accomplished with a single switch in the present invention.) Moreover, Layzell's crossbar array requires a number of switches an order of magnitude greater than the number of transistor terminals. (The present invention requires significantly less than that and in the disclosed embodiment requires no more reconfigurable switches than the number of transistor terminals.)

With these distinctions in mind, the present claims contain limitations that clearly distinguish over the cited references. Claim 1 requires plural transistors connected in series, power terminal to power terminal, each such connection being made through a single respective reconfigurable switch. The combination of Levi, Sourgen and Layzell fails to suggest such a limitation. Levi is unconcerned with reconfiguration at the transistor level. Sourgen discloses no reconfigurable switches at the power terminal to power terminal connections of series-connected transistors. Layzell's crossbar array requires the switching of at least two (or more) switches in the crossbar array to connect or disconnect the source of one transistor to or from the drain of another transistor (for example), so that Layzell cannot meet the limitation of a single switch effecting the connection/disconnection. Therefore, Claim 1 is patentably distinguished from the cited references based upon the claim language, "*each pair of successive transistors in said succession have a connection at the first power terminal of one transistor and the second power terminal of the other transistor of the pair through a corresponding single reconfigurable switch, each connection being governed by the corresponding single*

reconfigurable switch".

Independent Claim 10 requires that a single switch governs each terminal-to-terminal connection among the plurality of transistors AND that all such connections are through reconfigurable switches. Layzell cannot meet the first limitation while Sourgen cannot meet the second limitation, and there appears to be no way of combining Sourgen and Layzell to meet both limitations simultaneously, absent the hindsight of the present invention. In this regard, there appears to be no reason or advantage whatsoever to be gained from superimposing Layzells' crossbar array onto Sourgen's programmable rise time generator. The only motivation possible would appear to be impermissble hindsight of the applicants' invention.

Independent Claim 13 requires that a single switch governs each terminal-to-terminal connection among the transistors AND that the number of reconfigurable switches is close to the total number of transistor terminals in the array of transistors. Sourgen cannot meet the first limitation because his source-to-drain series connections are NOT governed by switches (they are permanent), while Layzell cannot meet the second limitation because of the large number of switches necessarily present in Layzell's crossbar array. Moreover, there appears to be no way of combining Sourgen and Layzell to meet both limitations simultaneously, absent the hindsight of the present invention.

An advantage is that with a smaller number of reconfigurable switches, an evolutionary algorithm can run more efficiently to convergence. There is nothing in the cited references suggesting that the number of switches can be so minimized. The only cited references concerned with evolutionary circuit synthesis, namely Levi and Layzell, contain no such suggestion. Levi is unconcerned with transistor level reconfiguration, while the number of reconfigurable switches required in Layzell's crossbar

is more than an order of magnitude greater than the number of transistor terminals. Sourgen is irrelevant to this feature because Sourgen has nothing to do with evolutionary circuit synthesis. Therefore, Claim 13 is patentably distinguished over the combination of cited references.

Independent Claim 16 specifies that the switches are held fixed in operation mode and are not fixed in a configuration mode for changing circuit topology, and each terminal-to-terminal connection is governed by a single reconfigurable switch. The combination of cited references cannot meet that combination of elements of Claim 13. Sourgen has nothing to do with changing circuit topology, since the functionality of Sourgen's programmable rising edge generator never changes to some other function. Therefore, his teachings would not be combined with evolutionary circuit synthesis of Levi or Layzell. Sourgen cannot meet the limitation of Claim 10 of, "*whereby one transistor is isolatable from another adjacent transistor*". Sourgen discloses only bypass switches that are connected in parallel with his transistors, so that none of his transistor-to-transistor connections can be interrupted to *isolate* transistors from one another. The transistors in his serial chain remain connected all together in series and in addition may be further connected in parallel, so they cannot be isolated from one another. Levi is unconcerned with transistor level reconfiguration. , Layzell's crossbar array is incapable of providing a SINGLE reconfigurable switch capable of effecting and interrupting a single terminal-to-terminal connection, contrary to the limitation "*each single one of said reconfigurable switches providing an individual interruptable terminal-to-terminal connection*".

In summary, Claim 16 requires the combination of, among other things, two features, namely all transistor-to-transistor

connections being interruptable by respective reconfigurable switches, and that each connection is connectable and interruptable by a single reconfigurable switch. This combination is not suggested by the cited references. Layzell's apparatus is incapable of realizing connection and disconnection of a given connection by a SINGLE switch because his circuit is based upon a crossbar array. Sourgen's apparatus has transistor-to-transistor connections that are permanent and cannot be interrupted. Levi is unconcerned with transistor level reconfiguration. It is respectfully submitted that there is no way to combine the teachings of Sourgen and Layzell to realize the combination of Claim 10.

Respectfully submitted,

Dated: Jan. 26, 2004

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope to: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on Jan. 26, 2004.

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